

FIG. 1 (Prior Art)

FIG. 2 (Prior Art)

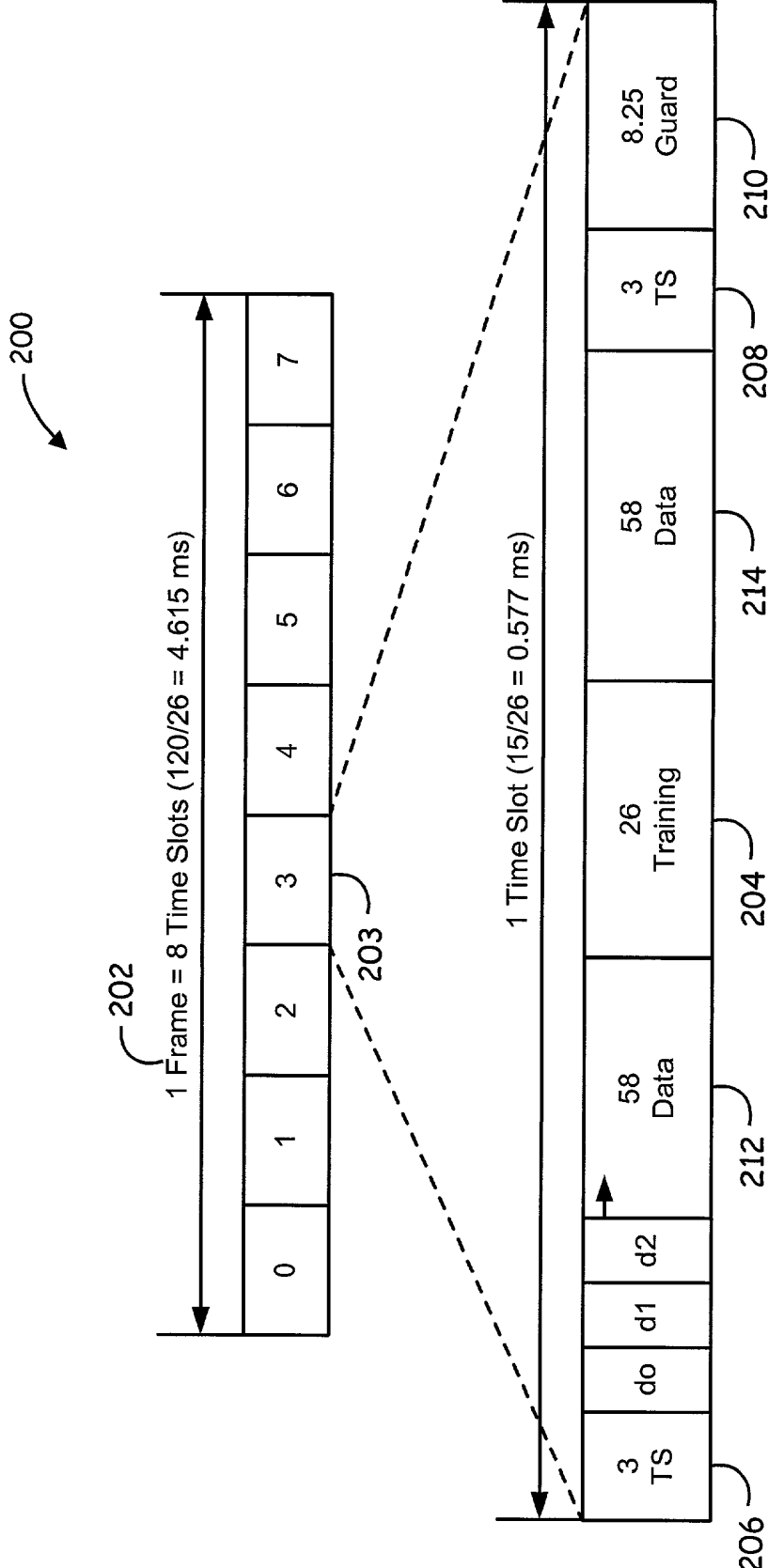


FIG. 2 (Prior Art)

FIG. 3 is a block diagram of a communication system 300. The system includes a Transmitter 304, a Channel 310, and a Receiver 320. Information Bits 302 are input to the Transmitter 304, which outputs a signal $s(t)$ to the Channel 310. The Channel 310 contains an $h(t)$ channel block 312 and a White Gaussian Noise block 314. The output of the $h(t)$ channel block 312 is added to the output of the White Gaussian Noise block 314 at a summing junction. The resulting signal is then received by the Receiver 320, which outputs Received Information Bits 322.

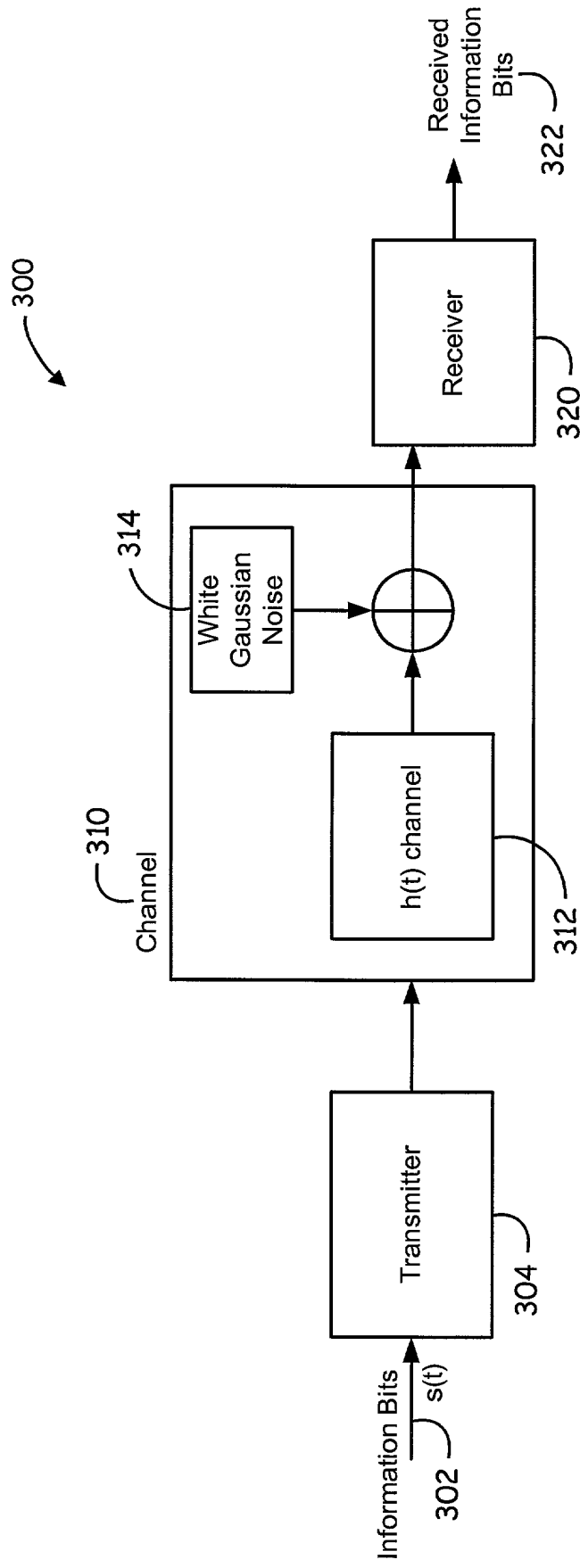


FIG. 3 (Prior Art)

FIG. 4 is a block diagram of a communication system 400. The system 400 includes a Frame Formatting block 402, a Channel Encoding and Puncturing block 404, an Interleaver block 406, a Burst Builder block 408, and a Modulator block 410. The blocks are connected in a sequential manner, with data flowing from left to right. The Frame Formatting block 402 outputs to the Channel Encoding and Puncturing block 404, which outputs to the Interleaver block 406. The Interleaver block 406 outputs to the Burst Builder block 408, which outputs to the Modulator block 410. The Modulator block 410 has an output arrow pointing to the right.

400

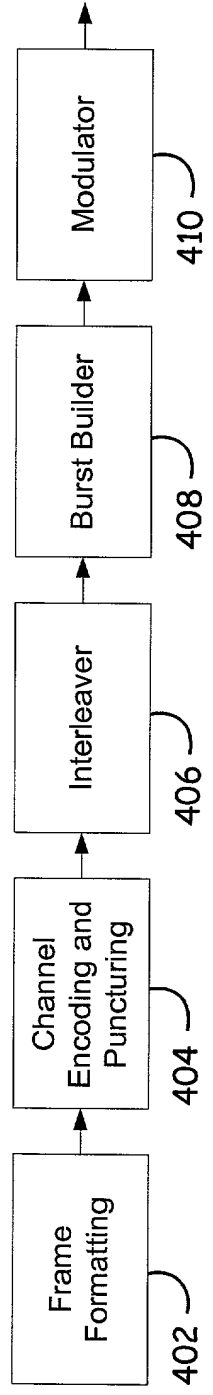


FIG. 4

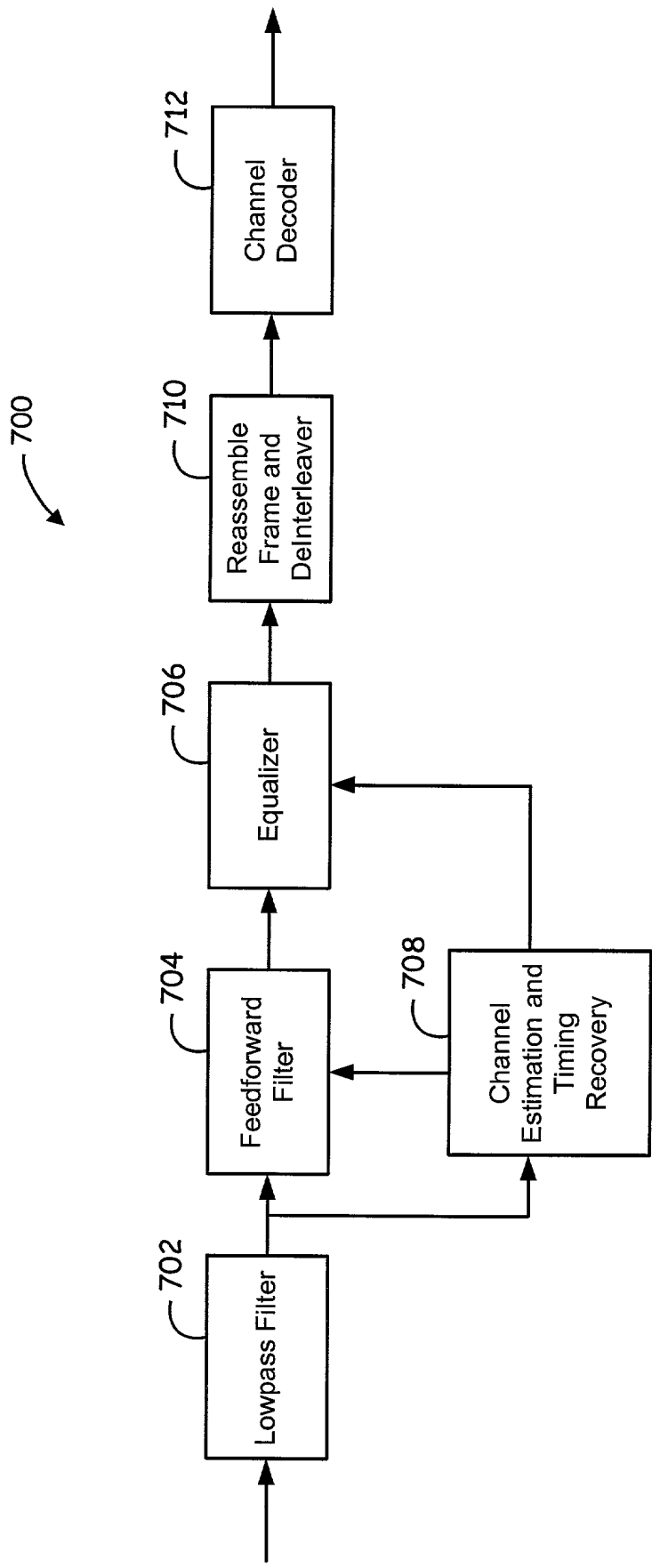


FIG. 7

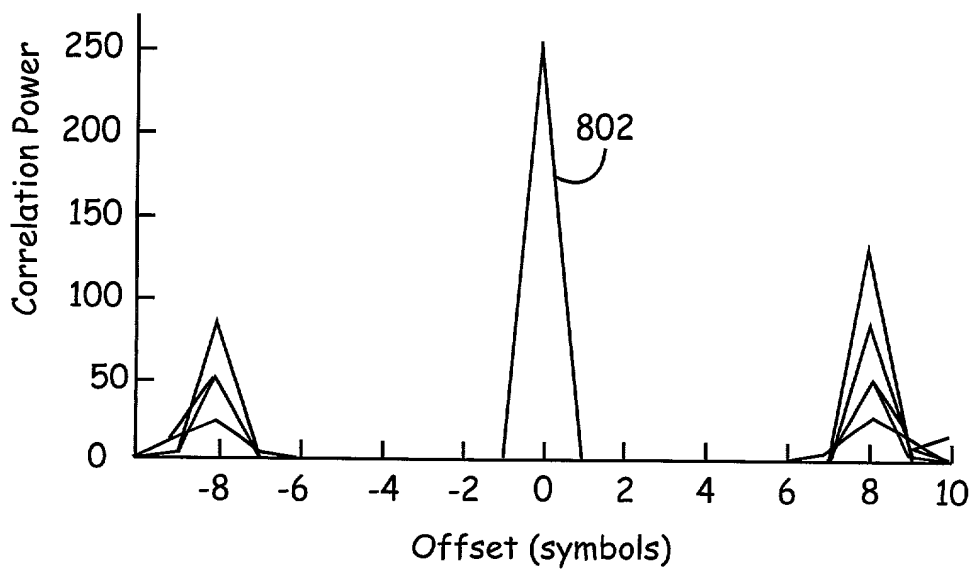


FIG. 8

FIG. 9 is a block diagram of a DFE (Decision Feedback Equalization) system 900. The system includes a Feed Forward Filter 902, a Feed Back Filter 904, a Decision Process 908, and a Feedback Filter 904. The system is configured to process an input signal and provide a feedback signal to the Feed Forward Filter 902.

DFE

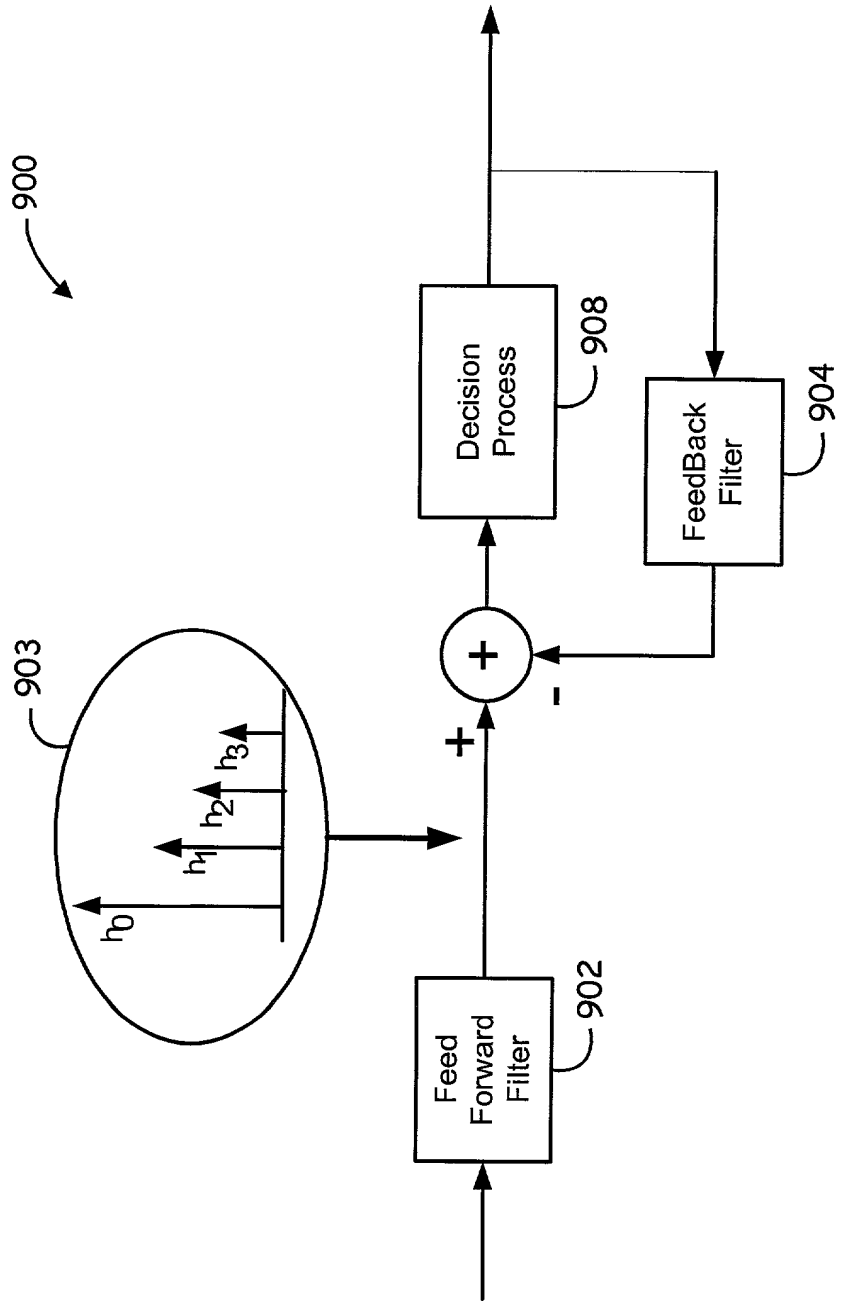


FIG. 9 (Prior Art)

FIG. 11 is a block diagram of a channel model 1100. The channel model 1100 includes a channel 1102 and a modulation 1104. The channel 1102 is represented by a sequence of taps h_0, h_1, h_2, h_3, h_4 . The modulation 1104 is represented by a sequence of states L_1, L, L . The equalizer complexity (States) is given by M^L .

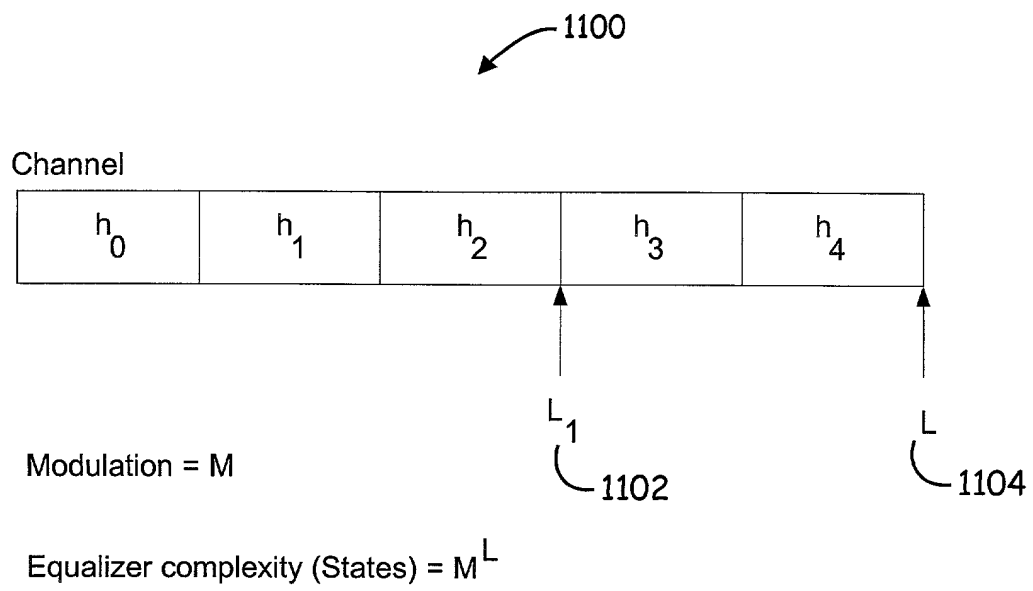


FIG. 11

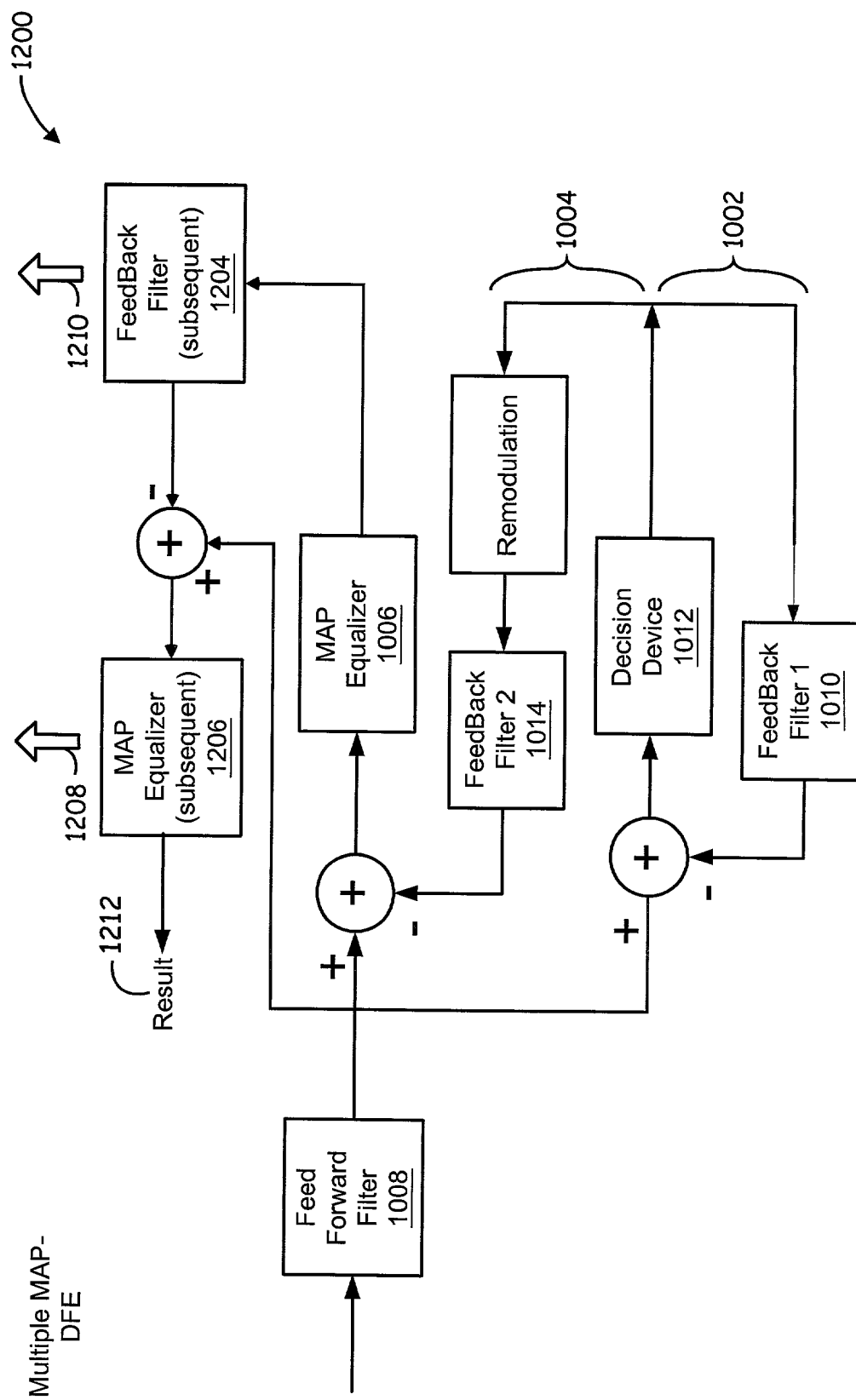


FIG. 12

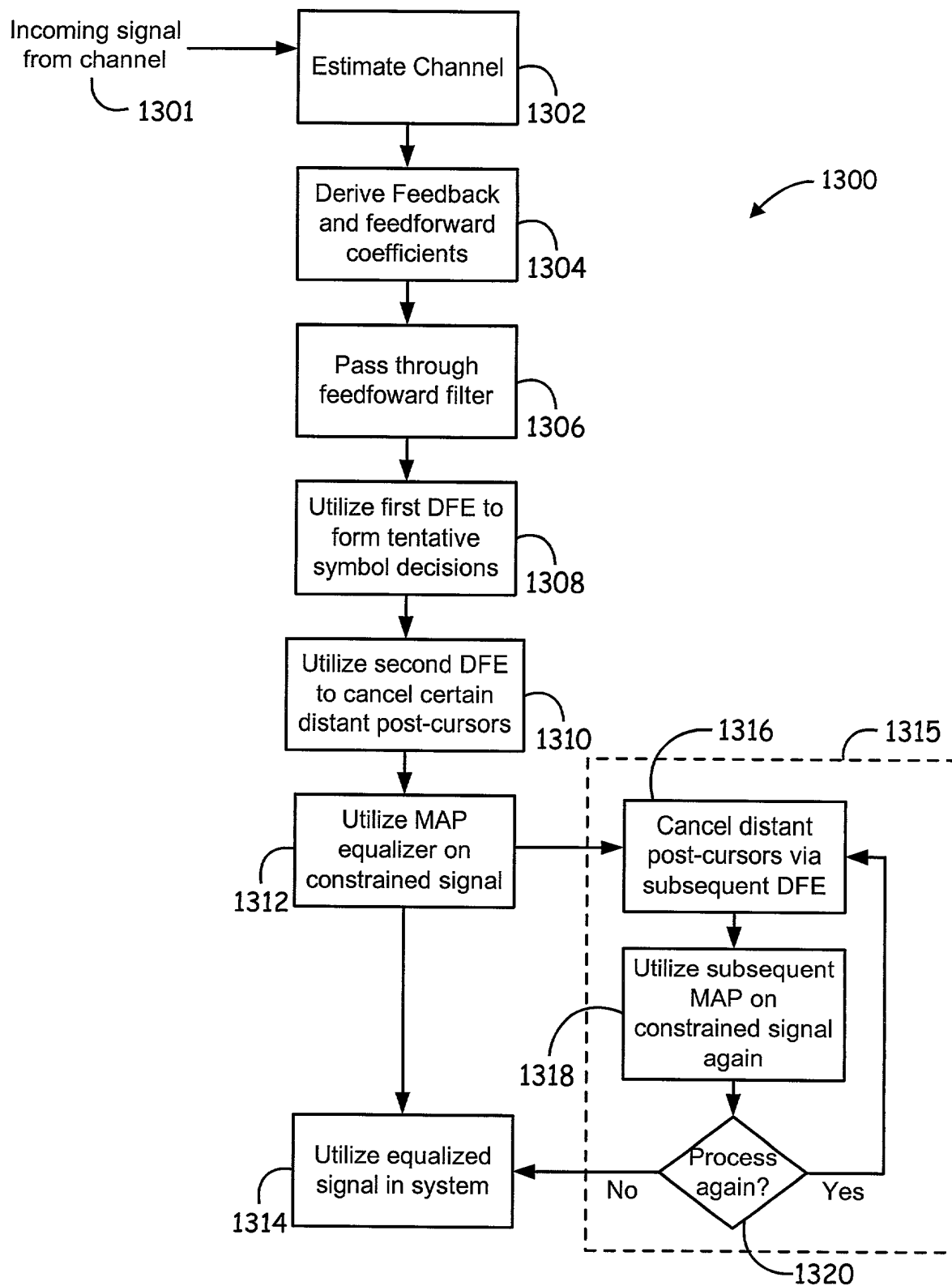


FIG. 13